The design methods of current-mode nth-order filters

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Index Terms:
active filters current conveyors current-mode circuits network synthesis CCII current conveyor current-mode high-order filter design filter circuits multi-output CC second-generation CC

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THE DESIGN METHODS OF CURRENT-MODE NTH-ORDER FILTERS

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Abstract: The design methods of nth-order filters by means of CC are studied, the filter circuits using CCII and MOCC are compared, and the merit and defect of two design methods are analyzed. The result states clearly that nth-order filter by means of MOCC has a small mount component and simple structure and has a bright future in the system of information processing.

Key words: Current conveyor, Active filters, Nth-order filters

电流模式 n 阶滤波器的设计方法

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摘 要： 研究用 CC 实现 n 阶滤波器的设计方法，通过比较用 CCII 和 MOCC 实现的滤波器电路，分析了两种不同设计方法的优劣。分析结果表明，用 MOCC 综合的 n 阶滤波器含有较少的元件，电路结构简单，在信息处理系统中有较好的使用前景。

关键词： 电流传送器，有源滤波器，n 阶滤波器

1. 引言

电流传送器（Current conveyor 简记为 CC）作为电流输出型有源器件在电路与系统中获得了广泛的应用，它可以简化电路结构、降低器件功耗、扩展工作频带，并具有很强的通用性和灵活性。利用电流传送器综合成的 n 阶有源滤波器具有功耗低、幅频特性好等特点，具有很广阔的使用价值。本文研究了利用第二代电流传送器（CCII）和多端输出电流传送器（MOCC）综合生成 n 阶有源滤波器的方法。

2. 电流传送器

2.1 CCII 电路结构 电流传送器是 60 年代末期出现的一种集成器件，CCII 是第二代产品，具有通频带宽、精度高、用途广等优点，其电路符号如图 1 所示，图中的+或-表示 CCII+或 CCII-，数学描述为：

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{1}$$

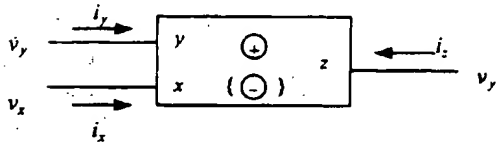

图 1 CCII 电路符号

2.2 MOCC 电路结构 MOCC 是多输出端电流传送器，其电路符号如图 2 所示，它具有正输出端 Z 和负输出端 Z，端口特性描述为：

$$\begin{bmatrix} i_y \\ V_x \\ i_{z1} \\ \vdots \\ i_{zm} \\ i'_{z1} \\ \vdots \\ i'_{zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ i_x \\ V_z \\ V_{\bar{z}} \end{bmatrix} \tag{2}$$

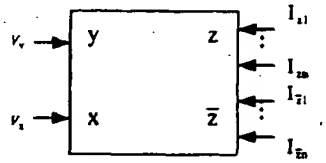

图 2 MOCC 电路符号

3. 用 CCII 实现 n 阶滤波器

n 阶滤波器电压传输函数为

$$H(s) = \frac{a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + a_0}{s^n + b_{n-1} s^{n-1} + \cdots + b_1 s + b_0} \tag{3}$$

相应的信号流图如图 3 所示。根据此信号流图，可以很容易地用 CCII 来实现 n 阶滤波器，具体电路如图 4 所示。

由图 4 可以看出，由 CCII 实现的 n 阶滤波器含有较多的元件，为了尽量简化电路结构，节省元件，可采用 MOCC 来实现 n 阶滤波器。

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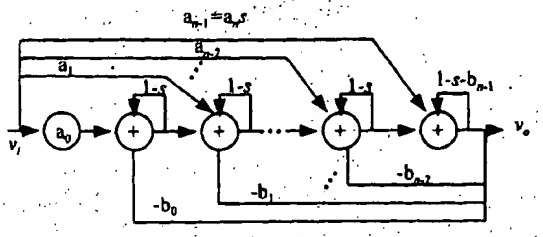

图 3　式（3）对应的信号流图

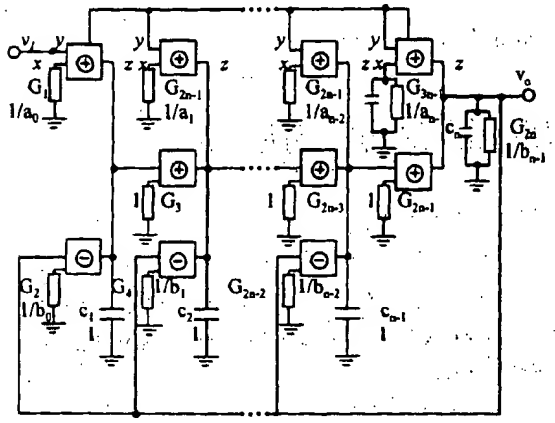

图 4　用 CCII 实现的 n 阶滤波器

4. 用 MOCC 实现 n 阶滤波器

由 MOCC 实现的 n 阶滤波器可以克服上述电路的不足，本文以 n 阶高通滤波器为例介绍 n 阶滤波器的设计方法。n 阶高通滤波器传输函数为

$$H(s)=\frac{as^n}{b_n s^n+b_{n-1}s^{n-1}+\cdots+b_1 s+1} \qquad (4)$$

其信号流图如图 5 所示。图中 k_j(j=0,1,...,n)为输入传输比例因子，$T_i=1/s\tau_i$（τ_i 为常数），参数间关系为

$\tau_n=b_1$，　$\tau_j=b_{n-j+1}$　　(j=n-1, n-2, ..., 1)

$k_0=a/b_n$，　$k_n=-\ k_0\ b_1\ b_{n-1}\ /b_n$

$$k_1=-k_0-\sum_{i=0}^{n-2}k_{n-i}$$

$$k_j=-\frac{b_{n-j}}{b_n}\left(k_0 b_{j-1}+\sum_{i=0}^{n-j-1}k_{n-i}b_{j+i}/b_{1+i}\right)$$

(j=n-1,n-2,...,2)　　(5)

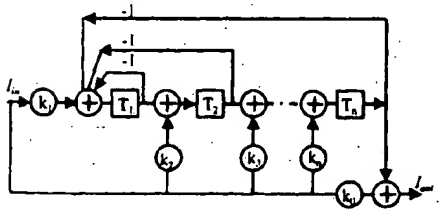

图 5　式（4）对应的信号流图

根据图 5 用 MOCC 实现的电路如图 6 所示，图中 $R_jC_j=\tau_j$，$R/R_0=k_0$。该电路只含有 n+1 个 MOCC，n 个接地电容和 n+2 个接地电阻，与图 3 相比较，大大减少了器件。

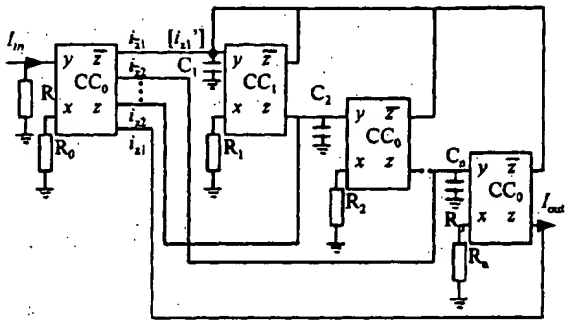

图 6　用 MOCC 实现的 n 阶高通滤波器

5. 设计举例

五阶巴特沃斯滤波器归一化传递函数为

$$H(s)=\frac{s^5}{s^5+3.236s^4+5.236s^3+5.236s^2+3.236s+1}$$

根据式（5）可求出以下参数：

$k_0=1$, $k_1=-5.003$, $k_2=4.004$, $k_3=-6.473$, $k_4=16.944$, $k_5=-10.472$, $\tau_1=0.309$, $\tau_2=0.618$, $\tau_3=1$, $\tau_4=1.618$, $\tau_5=3.236$。

实现此五阶滤波器的电路含有 6 个 MOCC，其中 CC_0 输出 Z 端有 3 个输出分支 i_{z1}, i_{z2}, i_{z3}，分别注入 I_{out}、C_2、C_4，CC_0 输出 Z 端有 3 个输出分支 i_{z1}'，i_{z2}'，i_{z3}' 分别注入 C_1、C_3、C_5。电路图可参见图 6，电路参数分别为：$R_1=1k\Omega$，$R_2=2.4\ k\Omega$，$R_3=2.7\ k\Omega$，$R_4=3.3\ k\Omega$，$R_5=5.4\ k\Omega$，$C_1=309pF$，$C_2=257pF$，$C_3=370pF$，$C_4=490pF$，$C_5=599pF$。

6. 结论

本文研究了用电流传送器实现 n 阶滤波器的设计方法，其中用 CCII 实现的滤波器含有的元件较多，而采用 MOCC 设计的 n 阶滤波器克服了其不足之处，本文通过实例综合了 5 阶高通滤波器。由于该电路结构简单，含有的元件少，且功耗低、频带宽，因而在信息处理电路中有很好的使用前景。

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Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications

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Abstract:
A novel current mirror (CM), suitable for operation at low voltage levels is presented. Th mirror has high input and high output voltage swings. Adaptive current biasing is introduced for minimising the effects of offset current. A compensation technique has been used to increase the bandwidth. This makes the CM structure attractive for portable, high frequency circuit applications. P-SPICE simulations, based on models for 1.2 μm technology, validate the operation of the proposed current mirror for currents from 1 to 500 μA with 1.2 GHz bandwidth

Index Terms:
CMOS analogue integrated circuits VLSI compensation current mirrors low-power electronics mixed analogue-digital integrated circuits 1 to 500 muA 1.2 GHz 1.2 micron HF circuit applications LV operation P-SPICE simulations adaptive current biasing bandwidth compensation technique high frequency circuit applications high input voltage swing high output voltage swing high performance current mirror low power current mirror low voltage current mirror offset current portable analogue applications portable mixed mode applications

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1 Introduction

The demand for portability has made low power usage a key factor in integrated circuit design. Low power circuits normally find use in both digital and analogue mobile systems. Non-mobile applications also prefer to have low voltage (LV) operation to eliminate instrument-cooling requirements.

A CM is a common building block both in analogue and mixed mode VLSI circuits. Almost all high impedance CMs reported so far [1–3] need high input voltages, which give them the capability of high output voltage signal swing. The input voltage requirement for these CMs depends solely on the threshold voltage (V_t) of the input MOSFET, thus making them unsuitable for low voltage operation. New low voltage CM (LVCM) circuits, therefore, need to be investigated for getting high signal swings at input and output terminals. A few CM topologies with reduced input voltage requirements have been reported in [4, 5], where either a level shifter or a bulk-driven approach [1] has been used. The CM proposed in [4] is capable of operating at a low supply of 1.3V, but it has limited current range (< 150μA) with a bandwidth of 100MHz. The CM proposed in [1] has limited current range (< 100μA), while that proposed in [5] is not suitable for high frequency applications.

A novel LVCM with adaptive biasing and high input and high output voltage swings is presented in this paper. Adaptive biasing enhances the input signal swing capability and reduces the undesirable offset current. The use of capacitive and resistive compensation gives a bandwidth of 1.2GHz. The proposed LVCM can operate at a bias voltage less than 1.2V for an input current less than 200μA; and less than 1.7V for input current ranging from 200 to 500μA with output impedance of approximately 1MΩ.

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2 LVCM topology

The simple CM topology shown in Fig. 1*a* requires input voltage (V_{in}) of at least one V_t, and is unsuitable for any LV applications. The modified CM (Fig. 1*b*), which operates at low voltage, incorporates a level shifter PMOS transistor M4 (biased through a current I_{bias1}) at input port. For this structure, we have

$$V_{ds1} = V_{gs1} - V_{gs4} \quad (1)$$

where V_{ds1} and V_{gs1} are the drain to source and gate to source voltages for M1. V_{gs4} is the gate to source voltage for M4.

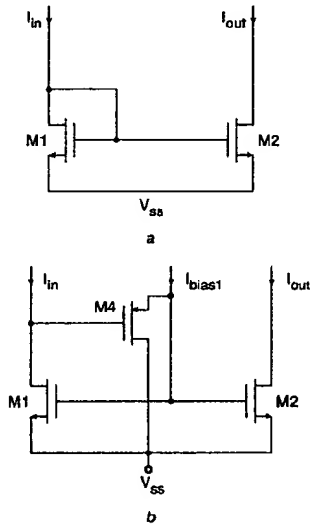

Fig. 1 *CM structures*
a Conventional CM structure
b Conventional level shifted CM structure

M4 is operated in sub-threshold region and V_{gs4} is approximately 0.6 V. It is required to have a minimum V_{gs1} equal to at least one V_t to operate M1 in either linear/

saturation region. If V_{ds1} equals 0.2V, then M1 operates in the saturation region. However, M4 operates in the sub-threshold region for the entire input current (I_{in}) range. The operation of M1 and M2 depends on I_{in} and their aspect ratios (W/L). Hence, when $I_{in} < 1.0\mu A$, M1 operates in the sub-threshold region and when I_{in} exceeds 1.0μA, M1 operates in the saturation region.

2.1 Operation in sub-threshold region

At low input currents, M1 and M2 operate in the sub-threshold regions and the input voltage present due to the injection of I_{in} is given by

$$V_{in} \simeq \eta V_T \left[\log \frac{I_{DO4}}{I_{DO1}} \frac{L_1}{L_4} \frac{W_4}{W_1} \frac{I_{in}}{I_{bias1}}\right] \quad (2)$$

where V_T is the thermal voltage. I_{DO1} and I_{DO4} are process parameters, (W/L) represents transistor aspect ratio, and η lies between 1.2 and 2.0.

As I_{in} increases, both M1 and M2 enter into the saturation region and the circuit analysis carried out in the following Sections assumes that M1 and M2 are in the saturation regions.

2.2 Proposed LVCM structure

The CM structures shown in Fig. 1 do not have high output resistance. The LVCM structure shown in Fig. 2 is based on the triode transconductor structure [6], and is expected to increase the output resistance. The input current I_{in} is pumped into the drain of M1. The bias current of M4 is kept small so that M4 operates in the sub-threshold region and M1 is in the saturation region. The transconductance (g_{m1}) and channel conductance (g_{d1}) of M1 decide the input impedance (R_{in}). Here, M4 provides the requisite gate bias for M1 and M2 while M5 provides suitable bias for M3. V_{in} is given by

$$V_{in} = \sqrt{\frac{2I_{in}}{\beta_1}} + \Delta V_{th} - \left|\eta V_T \ln\left(\frac{L_4}{W_4}\frac{I_{bias1}}{I_{DO4}}\right)\right| \quad (3)$$

where ΔV_{th} (= $V_{tp} - V_{tn}$) is the mismatch between the threshold voltages of M1 and M4 and β_1 represents the transconductance parameter for M1.

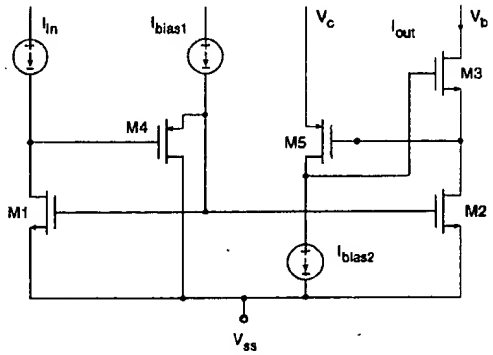

Fig. 2 *Proposed high output impedance LVCM*

V_{gs1} and V_{gs2} are equal, but V_{ds2} depends on the applied bias voltage (V_B), output current (I_{out}) and the bias current of M5 (I_{bias2}). We choose I_{bias2} to be 10μA, which ensures that M5 operates in the linear region for entire range of V_B because the drain gate voltage of M5 equals V_{gs3}.

For a current flow through M3 and M2, lower V_B implies lower V_{ds2}. This causes higher V_{gs5} than that required for I_{bias2} to flow. V_{ds5} depends on the gate bias of M3 and is at least equal to $V_{ds2} + V_{tn}$. These conditions ensure that M5 operates in the linear region. Also, V_{ds2} increases as V_B is increased and M3 has to pump I_{out} but drain source voltage of M3 is small and inadequate for the purpose. Hence, it requires higher gate source bias, which equals the difference of applied voltage at source of M5 (V_C) and the drain voltage of M2 (= $V_C - V_{ds5}$). V_C is normally taken as V_{DD} itself. Now, V_B divides between V_{ds2} and V_{ds3} as:

$$\frac{V_{ds2}}{V_{ds3}} = \frac{\beta_3(V_C - V_{ds2} - V_{tn})}{\beta_2(V_{ds1} + V_{gs4} - V_{tp})} \quad (4)$$

When V_B is small, the above ratio is high and V_{ds2} equals V_B. With the increase in V_B, V_{ds2} rises as M5 enters into the saturation from the linear region. When V_{ds2} increases further, V_{gs3} decreases to a minimum value where further decrease in V_{gs3} will not allow I_{out} to flow. Now the increase in V_{ds2} stops and remains fairly independent and V_{ds3} starts rising. M3 enters into saturation, resulting M5 to be always in the linear region.

The input impedance (R_{in}) and the output impedance (R_{out}) are given by

$$R_{in} \approx \frac{1}{g_{m1}} \quad (5)$$

$$R_{out} \approx \frac{g_{m3}}{g_{d2}g_{d3}} \quad (6)$$

where g_{d2} and g_{d3} represent the output conductances of M2 and M3, while g_{m1} and g_{m3} represent transconductances for M1 and M3, respectively. Similarly, the minimum output voltage necessary for CM operation is equal to:

$$V_{out}(\min) = V_{ds2}(\min) + V_{ds3}(\min) \quad (7)$$

3 Adaptive biasing technique

For the LVCM of Fig. 2, a minimum I_{bias1} is required and V_{in} is dependent of both I_{in} and I_{bias1}. If I_{in} is increased, then V_{in} also increases. But this increase can be reduced to a smaller value by increasing I_{bias1}. It is possible to increase I_{bias1} proportional to I_{in} by using the CMs obtained using M6, M7 and M8 (Fig. 3). The current through M8 is proportional to I_{in} and is I_{bias1}.

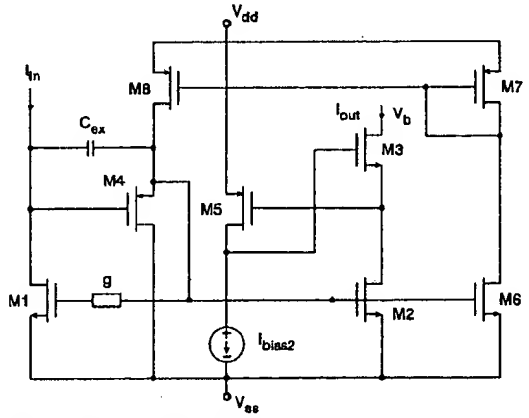

Fig. 3 *Proposed ABLVCM structure*

The gate source voltage for M2 (V_{gs2}) is given by

$$V_{gs2} = V_{ds1} + \left|\eta V_T \ln\left(\frac{L_4}{W_4}\frac{I_{bias1}}{I_{DO4}}\right)\right| + |V_{tp4}| \quad (8)$$

where V_{tp4} is the threshold voltage of M4.

We find that V_{gs2} depends on V_{ds1} and I_{bias1}. For low input current ($I_{in} \leq 1\mu A$), V_{ds2} is nearly equal to zero volts and I_{bias1} solely decides V_{gs2}. I_{bias1} drives V_{gs2} to be near V_{th} even for zero I_{in}. V_{in} will also be zero, but V_{ds2} increases independently with V_B. Under this condition, a current flows through M2 (even though I_{in} is zero), because I_{bias1} decides the gate bias for M2 and V_{ds2} increases independently with V_B. This condition drives M2 into the sub-threshold region and a small current, known as the offset current (I_{offset}), flows through M2. As I_{bias1} increases, the gate source bias of M2 increases, although V_{in} is still negligible ($\simeq 0.0$ V for $I_{in} < 1\mu A$). This causes I_{offset} to increase. Thus, I_{offset} restricts the increase in I_{bias1}.

Thus two contradictory requirements emerge (i.e. that I_{bias1} should be increased to keep V_{in} low and at the same time I_{bias1} should be decreased to keep I_{offset} low). In the design of an adaptively biased LVCM (ABLVCM), I_{bias1} is kept low, when I_{in} is low and is increased for higher I_{in}. Higher I_{bias1} imparts low V_{in} at higher I_{in} and lower I_{bias1} is necessary at low I_{in} to have low I_{offset}. Fig. 4 gives the values of offset current under different operating conditions.

We find that I_{offset} can also be minimised by matching the threshold voltages of the PMOS and NMOS transistors, but cannot be made zero. As shown in Fig. 4, operation of the PMOS transistor in the sub-threshold region reduces I_{offset} by a factor of 3. We have used this concept in the proposed ABLVCM structure.

4 Circuit modelling

The goal of circuit modelling is to obtain the functional relationship among the input and output variables, which depends upon some physical and bias parameters. Hybrid (h) parameters to model the small-signal behaviour for the LVCM are given in Fig. 5, where

$$C_{in} = C_{gd4} + C_{gs1} + C_{gd1} - \frac{g_{d4}(C_{gs4} + C_{gd1} + C_{ex})}{g_{m4}} \quad (9)$$

$$g_l = g + g\frac{C_{gs1}}{C_{gd1}} + g_{gd2} \quad (10)$$

$$C_p \approx C_{gs1} + C_{gs2} + C_{gs4} + C_{gd1} \quad (11)$$

$$C_x \approx C_p + C_{ex} \quad (12)$$

and g is the conductance connected between gates of M1 and M2.

5 Frequency enhancement

The high frequency response of the LVCM is described by the parameter h_{21} (Fig. 5). The addition of an external capacitor C_{ex} between the gate and source of M4 decreases the input capacitance C_{in} (eqn. 9) and increases C_x (eqn. 12). This results in shifting the pole-location away from the imaginary axis in the complex plane and the bandwidth decreases. But addition of g, as proposed in [7],

Parameter	Operating conditions	
	M1, M2, and M4 (in sub-threshold)	M1 and M2 (in sub-threshold) and M4 (in saturation)
I_{offset}	$\frac{W_2}{L_2}\frac{L_4}{W_4}\frac{I_{DO2}}{I_{DO4}} I_{bias1} \exp\left(\frac{\Delta V_{th}}{\eta V_T}\right)$	$\frac{\beta_2}{2}\left\{\sqrt{\frac{2I_{bias1}}{\beta_4}} + \Delta V_{th}\right\}^2$
I_{offset} (Minimum)	$\frac{W_2}{L_2}\frac{L_4}{W_4} I_{bias1}$	$\frac{K_2}{K_4}\frac{W_2}{L_2}\frac{L_4}{W_4} I_{bias1}$

Fig. 4 *I_{offset} under different operating conditions*

hybrid (h) parameters	Low frequency	High frequency
h_{11}	$\frac{g_{d4}}{g_{m1}g_{m4} + g_{d1}g_{d4}}$	$\frac{1}{g_{d1} + sC_{in}}$
h_{12}	0	0
h_{21}	$\frac{g_{m2}}{g_{m1}}$	$\frac{g_{m2}(g_l + g_{m4} + sC_x)}{(g_{d1} + sC_{in})(g_l + sC_x)}$
h_{22}	$\frac{g_{d2}g_{d3}}{g_{d2} + g_{d3}}$	$\frac{g_{d2}g_{d3}\left(1 + \frac{sC_{gd5}}{g_{d2}}\right)\left(1 + \frac{sC_{gs5}}{g_{d3}}\right)}{(g_{d2} + g_{d3})\left(1 + \frac{s(C_{gd5} + C_{gs5})}{g_{d2} + g_{d3}}\right)}$

Fig. 5 *Hybrid (h) parameters*

increases g_l. This compensates for increase in C_x. When $g_l >> g_{m4}$, h_{21} reduces to following:

$$h_{21} \simeq \frac{g_{m2}}{g_{d1} + sC_{in}} \tag{13}$$

We find that C_{in} primarily decides the bandwidth of ABLVCM if g_{d1} is constant. Reducing C_{in} can increase the bandwidth of ABLVCM. This is achieved by addition of the external capacitance C_{ex}.

6 Sensitivity analysis

Sensitivity analysis of the CM is carried out to find the variation of the output current (I_{out}) for the variations in various critical device parameters. I_{out} is given by

$$I_{out} = \frac{\mu C_{OX} W}{2L} \times \left[V_{ds1} + \left| \eta V_T \ln \left(\frac{L_4}{W_4} \frac{I_{bias1}}{I_{DO4}} \right) \right| + |V_{tp4}| - V_{tn2} \right]^2 \tag{14}$$

The sensitivity of I_{out} was evaluated with respect to various parameters. The following observations are made from the sensitivity calculations.

For V_{ds2} less than 2.0V, the sensitivity of the output current to V_{ds2} change is almost negligible. Any variations occurring in the transistor dimensions (W and L) have immediate reflection on I_{out}. The sensitivity of I_{out} to I_{bias1} change is almost negligible and the sensitivity of I_{out} to the threshold voltage change is quite high, as is expected from any CM structure.

To calculate sensitivity of I_{out} to I_{in}, we assume $K_1 = K - \Delta K$, $K_2 = K + \Delta K$, $V_{t1} = V_t - \Delta V_t$ and $V_{t2} = V_t + \Delta V_t$. The current I_{out} is given by

$$I_{out} = \frac{\beta_2}{2} \left(\sqrt{\frac{2I_{in}}{\beta_1}} - 2\Delta V_t \right)^2 \tag{15}$$

For $\beta_1 = \beta_2$ we get

$$S_{I_{in}}^{I_{out}} \approx 1 - \frac{\Delta K}{K} \tag{16}$$

and the sensitivity of I_{out} to I_{in} is dependent on variation in K.

7 Temperature dependence

Several of MOSFET parameters such as mobility (μ) and the threshold voltage (V_t) are temperature dependent and their effects on CM performance need to be evaluated. For the ABLVCM under consideration, I_{out} is given by

$$I_{out} = \mu(T_0) T^{-3/2} \frac{C_{OX} W_2}{2L_2} \times \left[V_{ds1} + \frac{nkT}{q} \ln \left(\frac{L_4}{W_4} \frac{I_{bias1}}{I_{DO4}} \right) + \Delta V_{th} \right]^2 \tag{17}$$

Assuming the temperature changes in ΔV_{th} to be zero, the fractional temperature coefficient (TC_f) is given as

$$TC_f(I_{out}) = \frac{-1.5}{T} + \frac{2K_2 \frac{nk}{q} \frac{W_2}{L_2} \ln \left(\frac{L_4}{W_4} \frac{I_{bias1}}{I_{DO4}} \right)}{g_{m2}} \tag{18}$$

where $K_2 = \mu C_{OX}$ for M2. ABLVCM can be made temperature insensitive by selecting various parameters. If (L_4/W_4) is small and $I_{DO4} >> I_{bias1}$, we have

$$TC_f(I_{out}) = \frac{-1.5}{T} \tag{19}$$

This gives quite low TC_f (I_{out}), equal to 500ppm/°C at room temperature.

8 Simulation results

The parameters such as R_{in}, R_{out}, bandwidth and I_{offset}, which should be bias insensitive, decide the performance of the ABLVCM. The CM should also have high input and output voltage swing capabilities. The circuits have been simulated using level 3 SPICE parameters for 1.2μm technology with supply voltage of ±1V. The (W/L) ratios for various MOSFETS are given in Table 1.

Table 1: Aspect ratios

Device number	Type	Aspect ratio (W μm/l μm)	Figure number(s)
M1, M2	NMOS	84/2.4	2, 3
M3	NMOS	60/1.2	2, 3
M4, M5	PMOS	18/1.2	2, 3
M6	NMOS	8.4/2.4	3
M7	PMOS	120/1.2	3
M8	PMOS	2.4/4.8	3

8.1 LVCM

P-SPICE simulations were carried out for I_{bias1} and I_{bias2} of 100pA and 10μA respectively, for I_{in} between 1μA and 500μA. Input voltage (V_{in}) is plotted in Fig. 6 for various values of I_{in}. V_{in} required is 0.8V as against 1.36V for conventional CM for 500μA of I_{out}. This voltage is still higher for low voltage CM applications. For I_{out} < 200μA, the circuit operates with V_{in} < 0.5V. The variation of V_{in} as

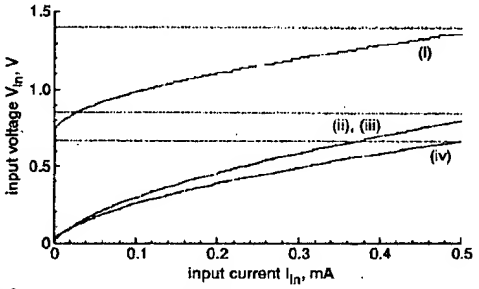

Fig. 6 *V_{in} against I_{in} characteristics*
(i) Conventional CM; (ii) simple CM structure; (iii) proposed LVCM structure; (iv) proposed ABLVCM

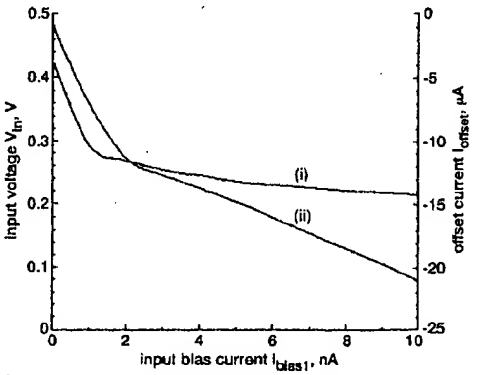

Fig. 7 *V_{in} developed at the input port for I_{in} = 100μA and I_{offset} characteristics as a function of I_{bias1}*
(i) Input voltage (V_{in}); (ii) offset current (I_{offset})

a function of I_{bias1} is shown in Fig. 7 for I_{in} of 100μA (trace (i)). Variation of I_{offset} as a function of I_{bias1} is also shown (trace (ii)). There is an I_{offset} of 5μA for I_{bias1} of 1nA and any decrease in I_{bias1} needs a higher V_{in} with reduced I_{offset}. I_{out} as a function of V_B for different values of I_{in} is given in Fig. 8, where I_{offset} is visible, when I_{in} is less than 10μA (inset of Fig. 8).

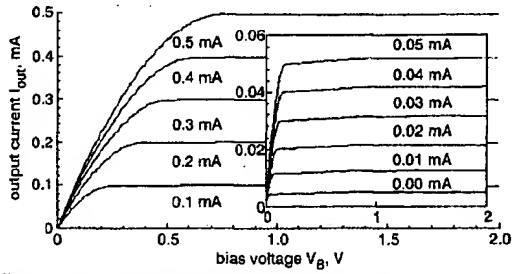

Fig. 8 *Current–voltage characteristics for proposed LVCM*
Figure in inset shows I–V characteristics at low currents

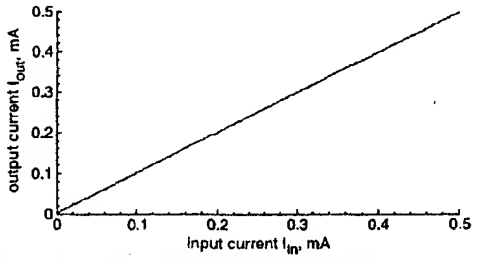

Fig. 9 *Current transfer characteristics of proposed LVCM*

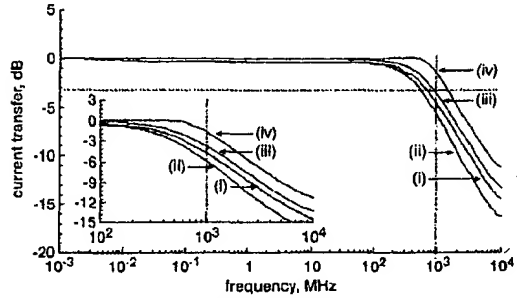

Fig. 10 *Frequency response of proposed LVCM*
(i) Without compensation; (ii) with resistive compensation; (iii) with capacitive compensation; (iv) with resistive and capacitive compensation
Figure shown in the inset depicts the expanded characteristics near cutoff frequency

We find that I_{out} to I_{in} ratio is almost equal to 1 (Fig. 9). The bandwidth is strongly dependent on the type of compensation used (as in Fig. 10 for I_{in} of 500μA). The bandwidth is about 630MHz (trace (i)) with no compensation. With addition of gate resistance, bandwidth reduces to approximately 500MHz (trace (ii)). There is a sag in the frequency response around 10kHz due to the presence of a zero around this frequency. Compensating capacitor increases the bandwidth to 790MHz (trace (iii)). With both external capacitor and resistance, the bandwidth increases twofold to 1.2GHz (trace (iv)) and the sag also disappears due to cancellation of zero by the addition of pole. The corresponding bandwidth for conventional CMs was found to be 550MHz (Fig. 1*a*), and 382MHz (Fig. 1*b*) and sag was also present.

8.2 ABLVCM

The ABLVCM uses adaptive biasing and frequency enhancement techniques. R_{in} and R_{out} are found to be 1.8kΩ and 1MΩ, respectively, at a supply voltage of ±1V. The sensitivity analysis of I_{out} with respect to the changes in the bias currents and bias voltages indicates that the variations in I_{out} are negligible.

The I_{in} against V_{in} characteristics for ABLVCM is also shown in Fig. 6. We find that V_{in} is 0.65V for I_{in} of 500μA, whereas it was 0.8V and 1.36V for the LVCM and the conventional CM, respectively. Fig. 11 is the plot of bias voltage against I_{out} for different values of I_{in}. I_{offset} is less than 1μA (inset of Fig. 11). It requires an output voltage less than 0.4V for I_{in} up to 200μA and approximately 0.65V for I_{in} up to 500μA.

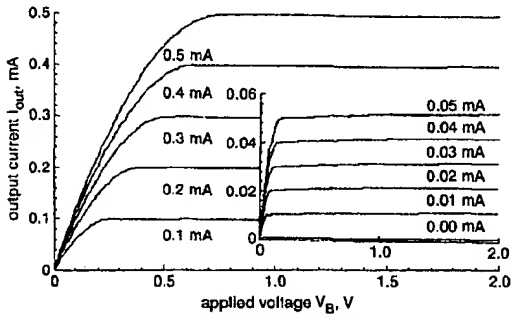

Fig. 11 *Current–voltage characteristics for proposed ABLVCM*
Figure in the inset shows I–V characteristics at low currents

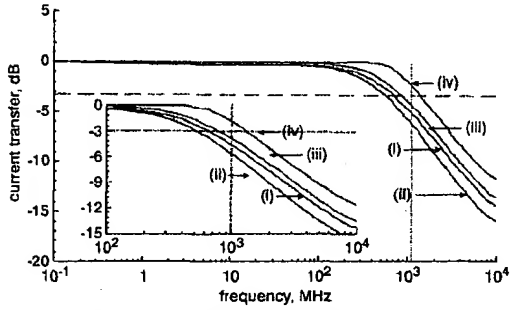

Fig. 12 *Frequency response of proposed ABLVCM*
(i) Without compensation; (ii) with resistive compensation; (iii) with capacitive compensation; (iv) with resistive and capacitive compensation
Figure shown in the inset shows the expanded characteristics near cutoff frequency

The frequency response of ABLVCM is similar to that of the LVCM and the bandwidth is dependent on the type of compensation used (Fig. 12). The bandwidth with and without compensation is the same as in the LVCM. Simulations shows that the bandwidth was 90MHz, 150MHz, and 210MHz for ABLVCM; 95MHz, 150MHz, and 200MHz for the CM of Fig. 1*a*; and 2kHz, 115MHz, and 140MHz for the CM of Fig. 1*b*, respectively, when I_{in} equals 10μA, 30μA and 50μA, respectively.

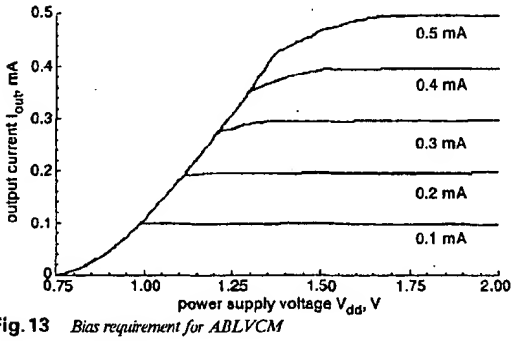

Fig. 13 *Bias requirement for ABLVCM*

Simulations were also carried out under different supply voltages to define the bias requirements (Fig. 13). For currents less than 400μA, the circuit performs satisfactorily at a single supply of 1.5V. However, bias voltage of more than 1.6V is needed for I_{in} more than 400μA.

The bandwidth of the proposed circuit was evaluated by simulating it at different voltage levels from ±0.625V to ±1.0V at I_{in} of 200μA. The bandwidth of the ABLVCM was independent of bias voltage when the latter is more than ±0.75V and was approximately 790 MHz. However for voltages less than ±0.75V, the bandwidth falls to 620MHz at ±0.625V. Worst-case analysis was carried out to find variations in I_{out} for 50% Gaussian deviations in the model parameters chosen for MOSFETs. The absolute error present in the DC current transfer is almost negligible for changes in model parameters (3μA at 120μA). The error in AC current transfer is also negligible. The bandwidth of the ABLVCM decreases by 5% over a temperature change from 0 to 100°C.

8.3 Comparative performance

We observe that the ABLVCM has better performance than other circuits. It operates satisfactorily with input voltage as low as 0.65V for current up to 500μA, whereas the other LVCM require more than 0.8V (Figs. 6, 8 and 11). It has quite low offset current. A supply voltage of 1.5V is needed to ensure proper bias requirement for M4 and M5; but other structures require higher voltage.

9 Conclusion

A novel high performance CMOS LVCM, which can operate with a supply voltage of 1.5V, is presented. The ABLVCM has wide input current range 1μA to 400μA at 1.5V with rail-to-rail input and output voltage swing. At 2V, the ABLVCM can operate up to 500μA. It has high bandwidth of approximately 1.2GHz. One immediate application is in the design of handheld equipment, where supply voltage and current are parameters of prime importance. This circuit can find wide-ranging applications in portable equipment, where analogue and mixed mode circuits are used.

10 Acknowledgment

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